

Multi-Slice Network Processor
Devanagondi, et al.
U.S. Serial No.: 10/612,889
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Replacement Sheet

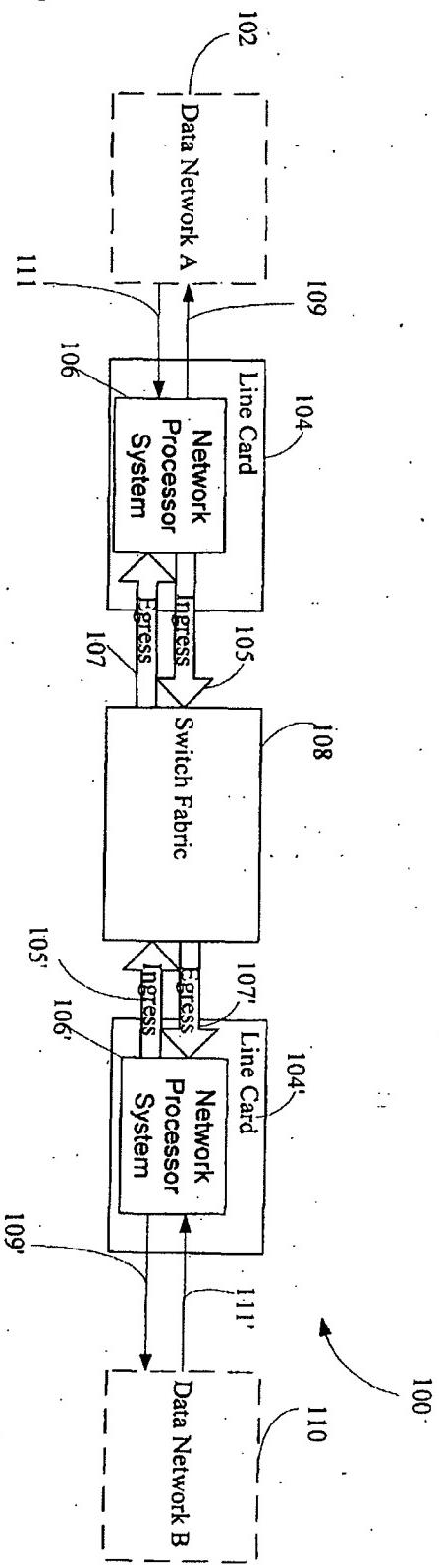


FIG. 1

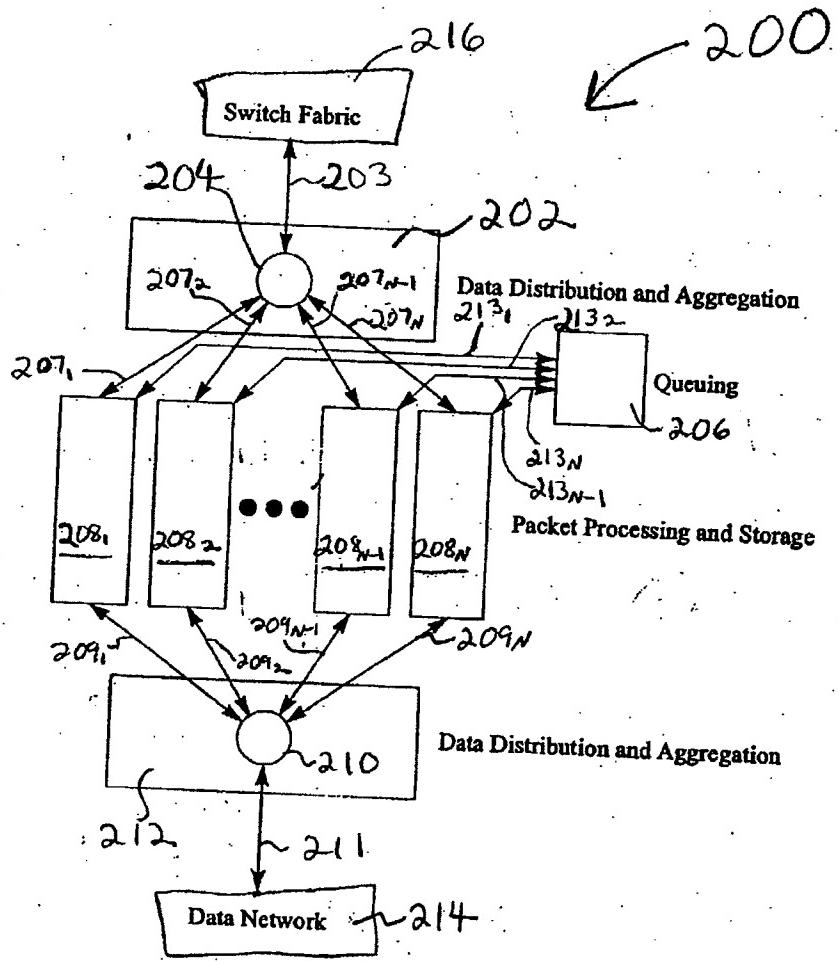


FIG. 2

Multi-Slice Network Processor

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FIG. 3

300

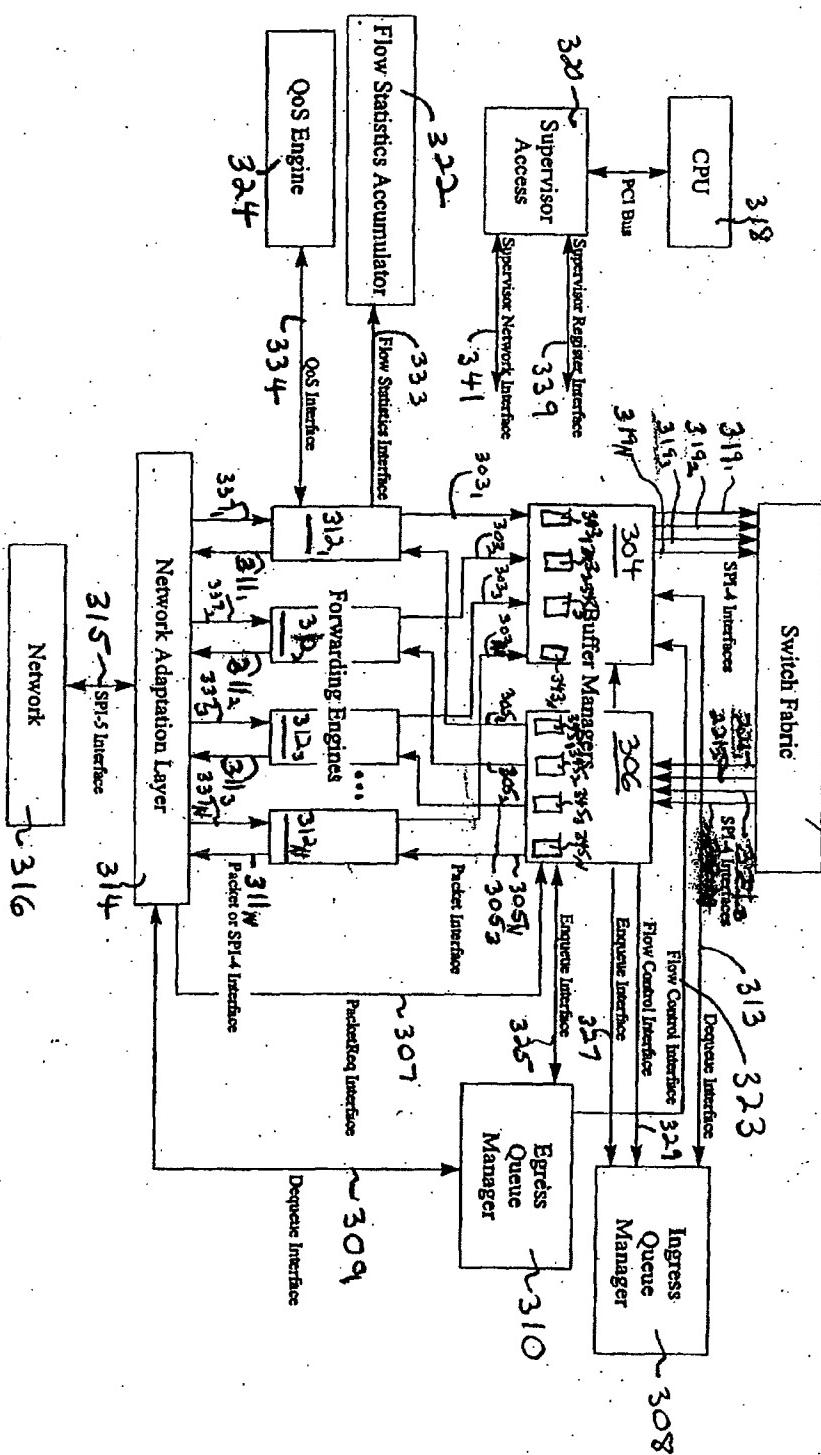


FIG. 4A

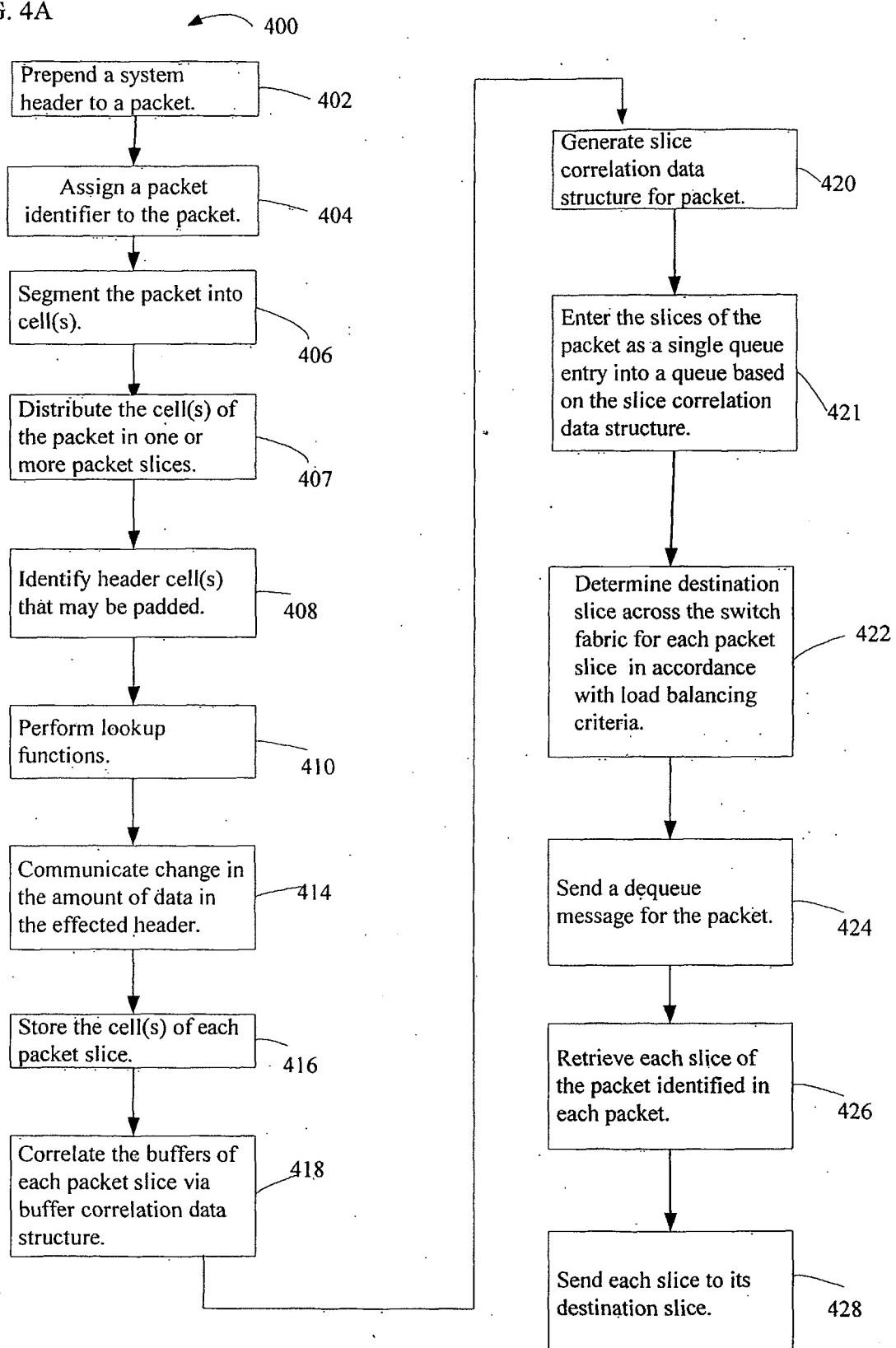


FIG. 4B

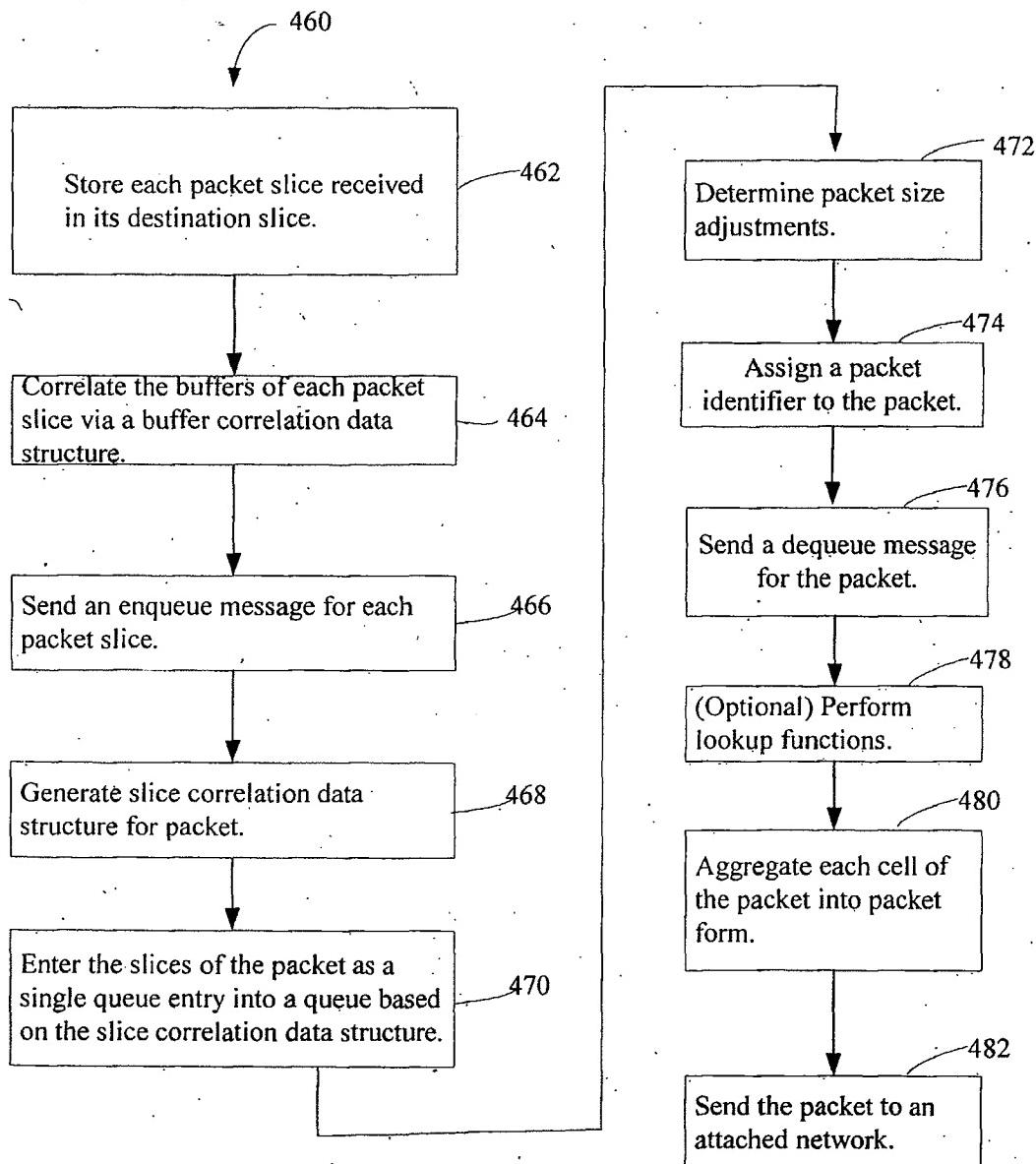
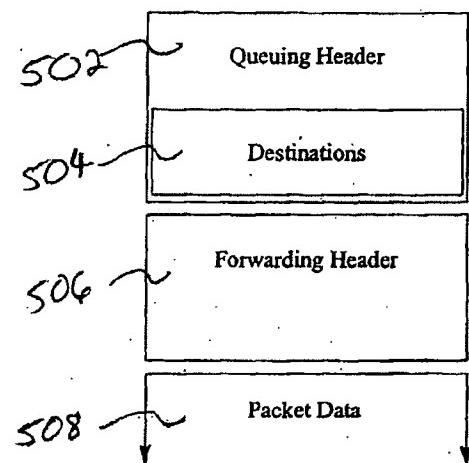


FIG. 5



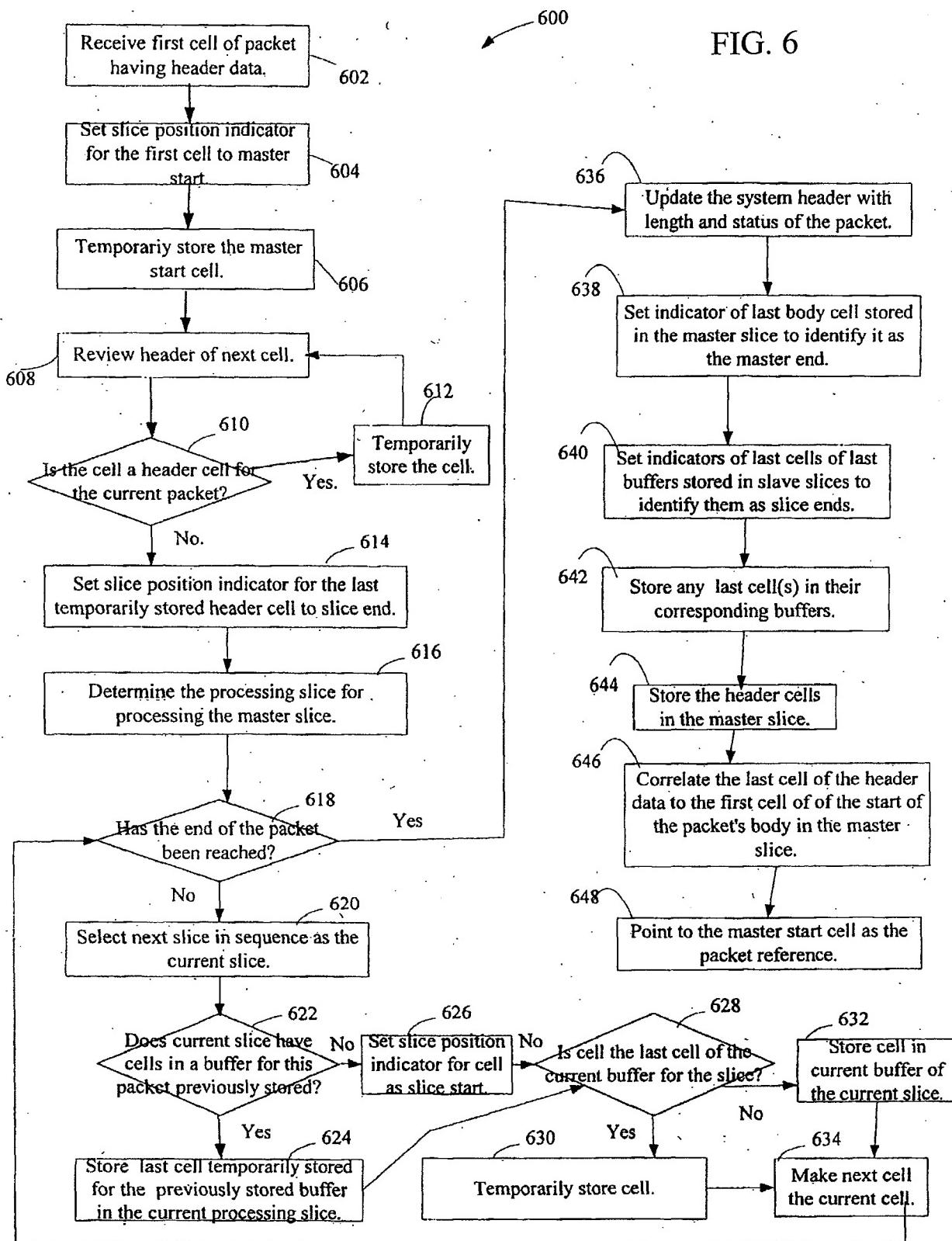


FIG. 6

Multi-Slice Network Processor

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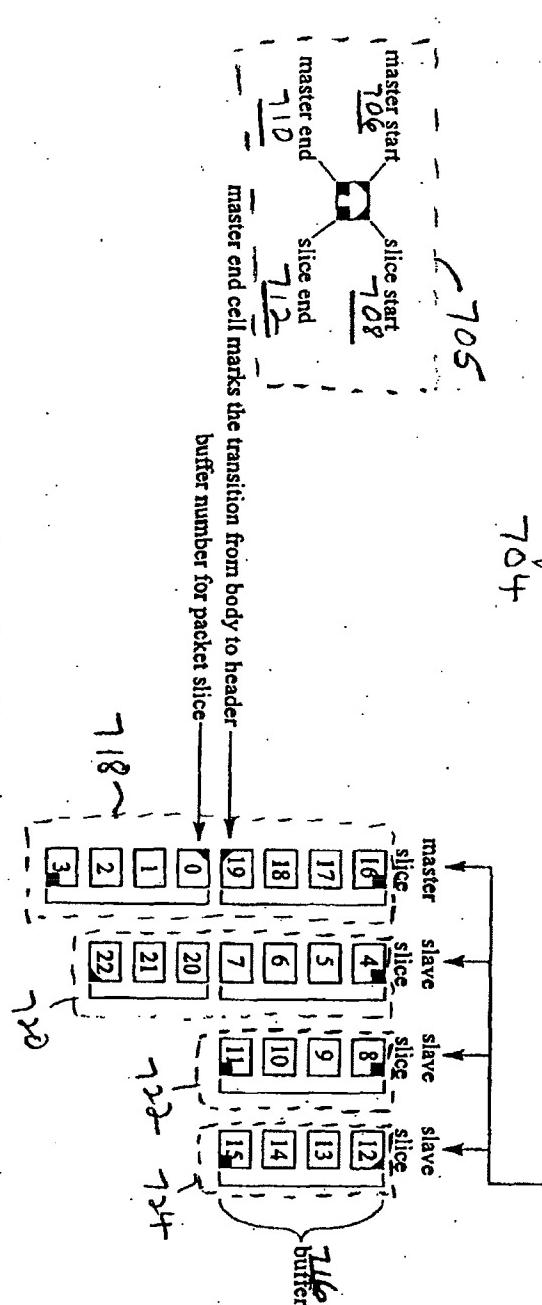
Packet cells as received from the network:

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

3	2	1	0	19	15	11	22	21	20	7	18	17	16	14	13	12	10	9	8	6	5	4
---	---	---	---	----	----	----	----	----	----	---	----	----	----	----	----	----	----	---	---	---	---	---

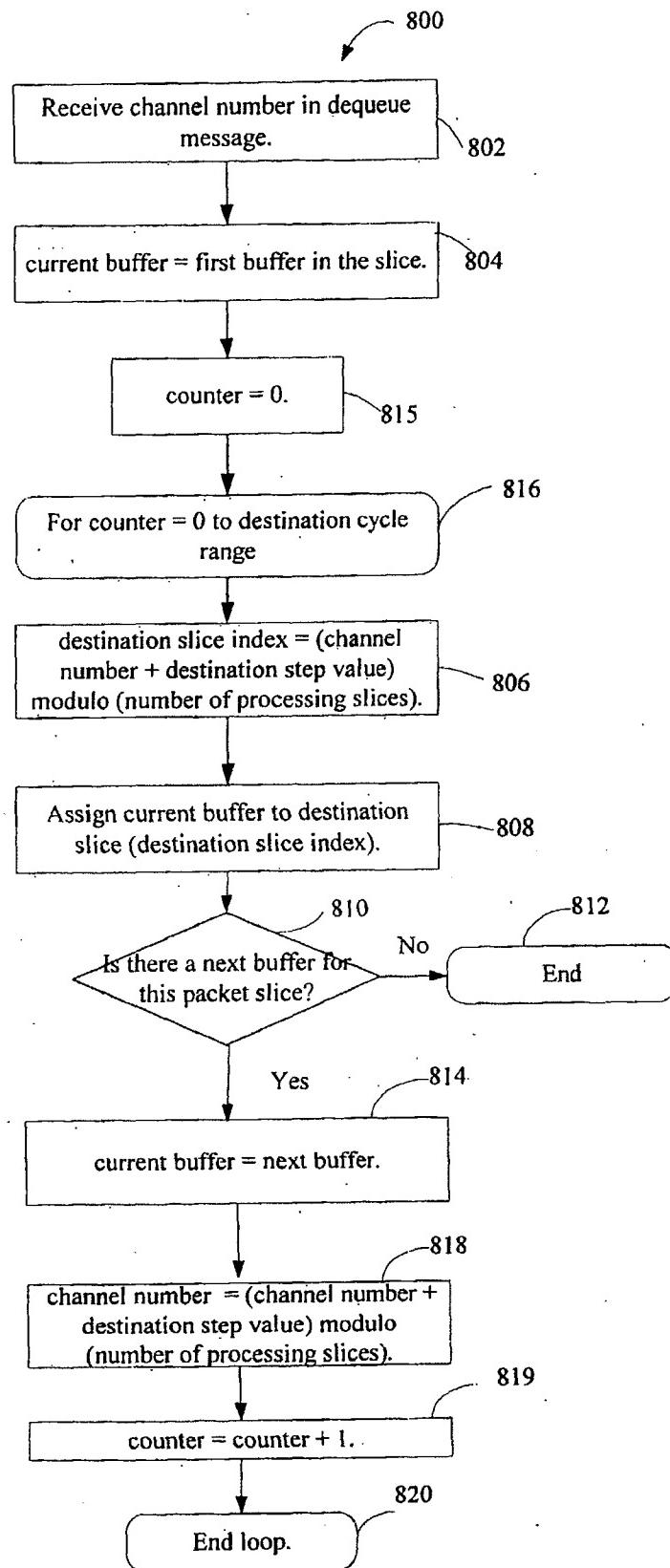
packet cells as delivered to the Forwarding Engines:

705	704	703	702	701	700	705	704	703	702	701	700	705	704	703	702	701	700	705	704	703	702	701	700
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----



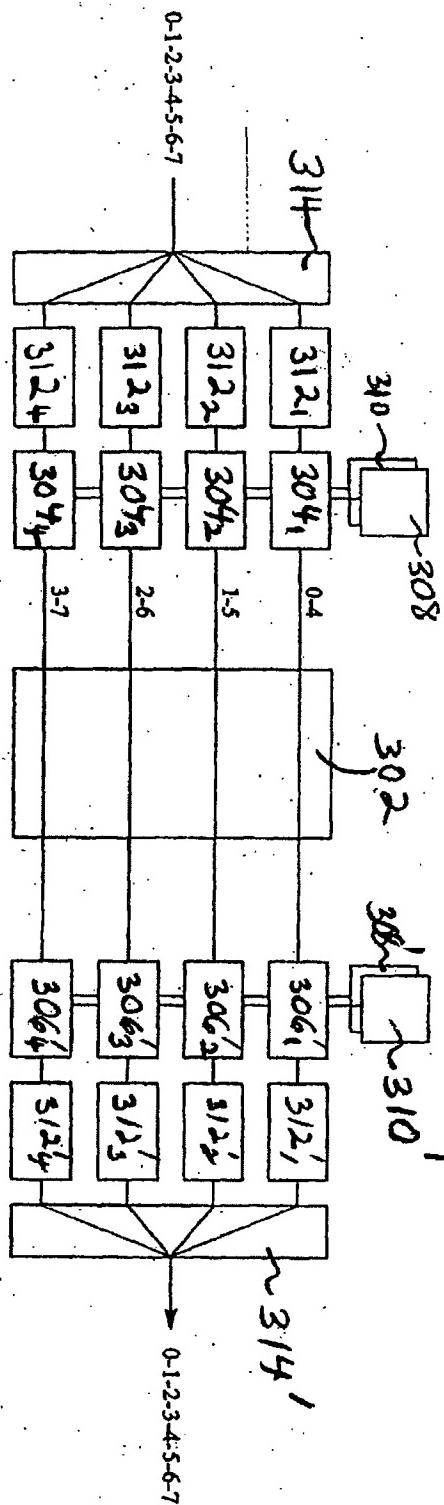
F16.7

FIG. 8



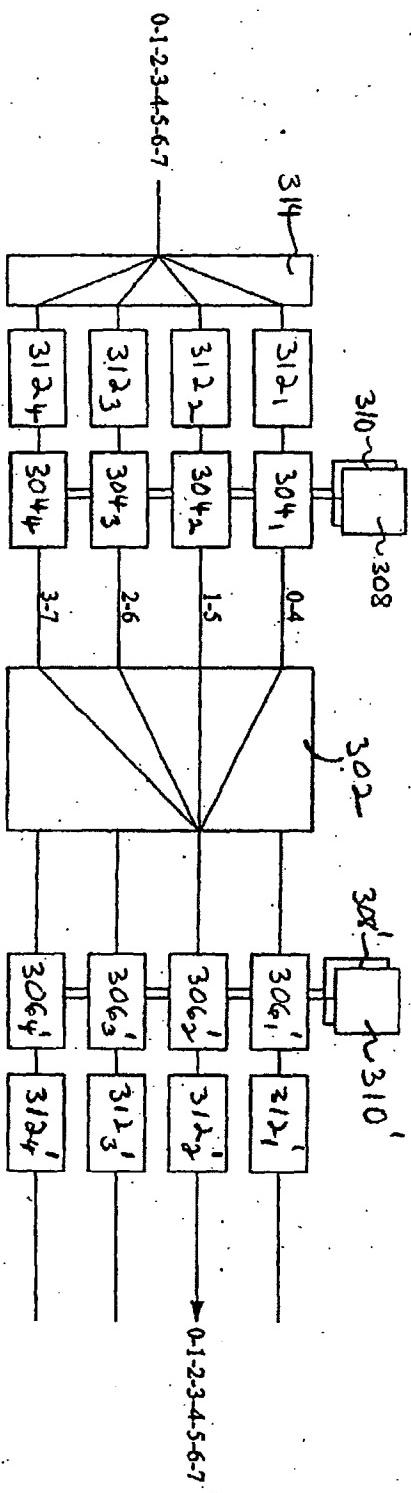
High Speed to High Speed Example

F 16. 9 A



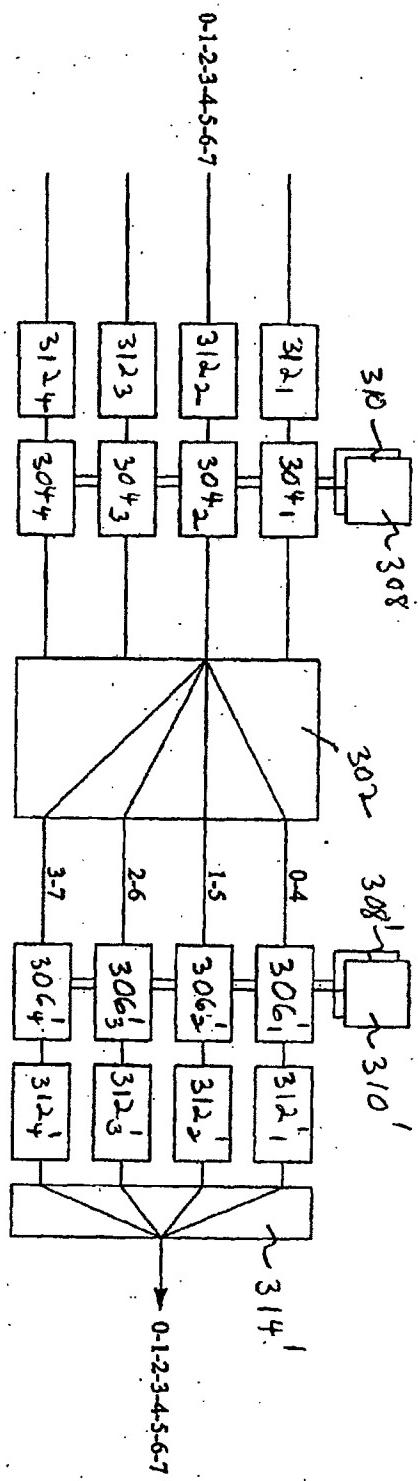
High Speed to Low Speed Example

F 16. 9 B

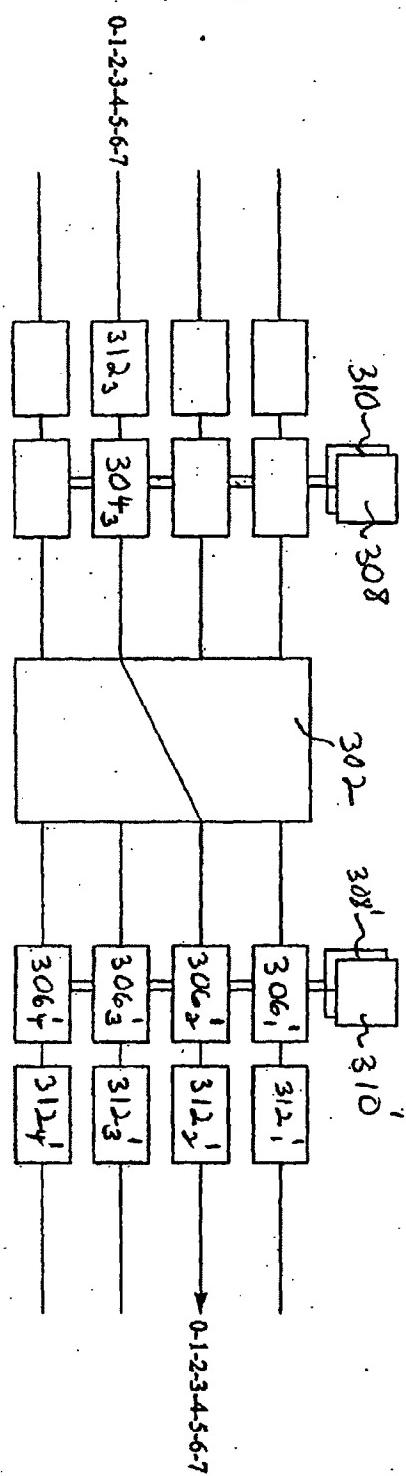


Low Speed to High Speed Example

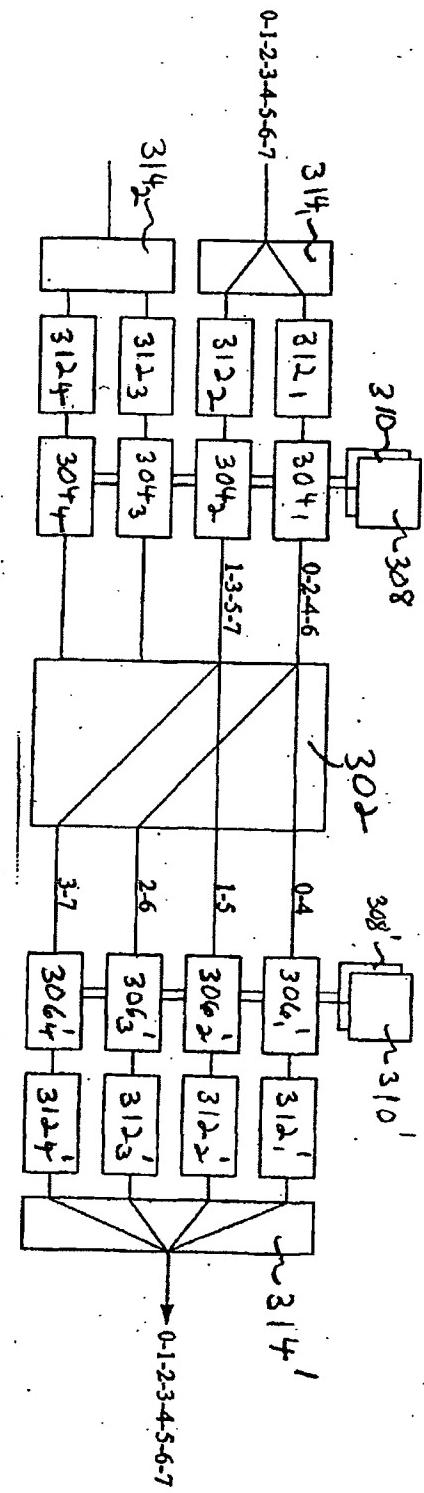
F 16. 9C



Low Speed to Low Speed Example F 16. 9D

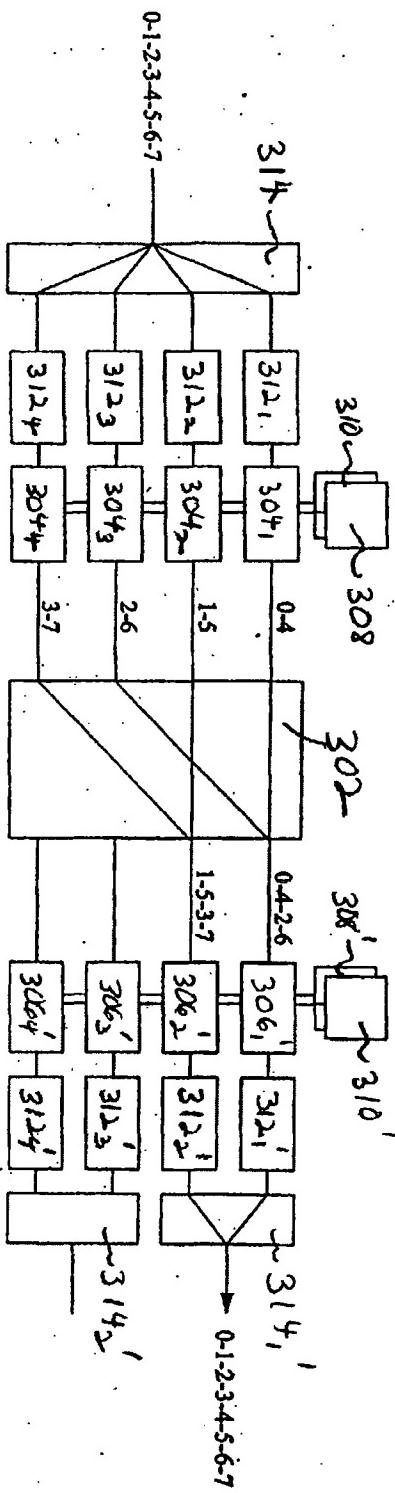


Medium Speed to High Speed Example F 16. 9 E



High Speed to Medium Speed Example

F 16. 9 E



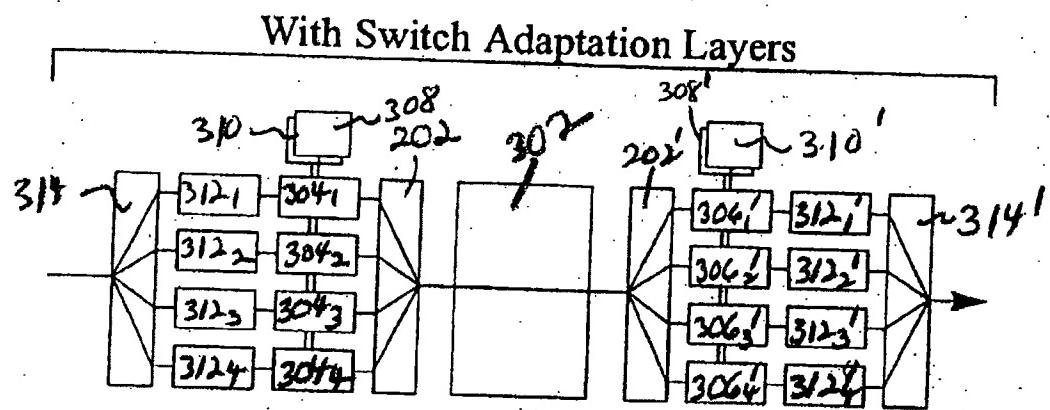
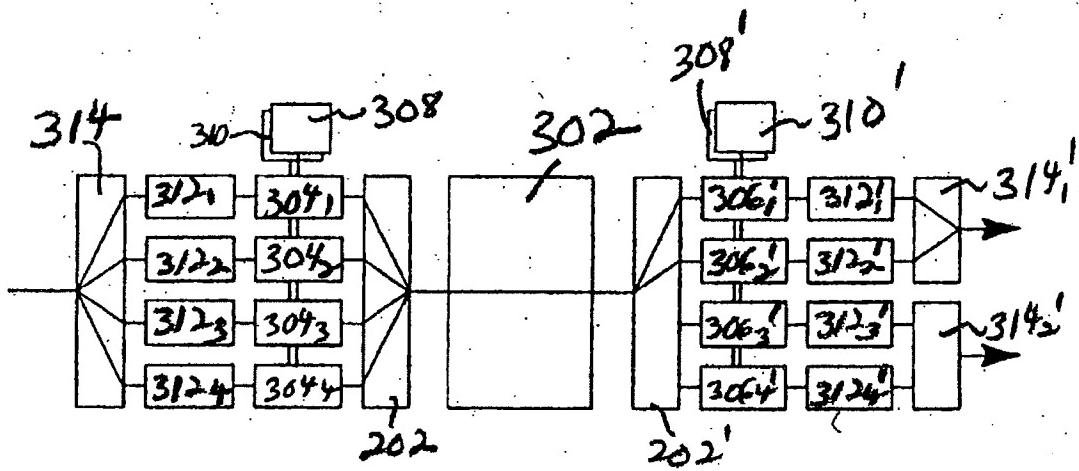


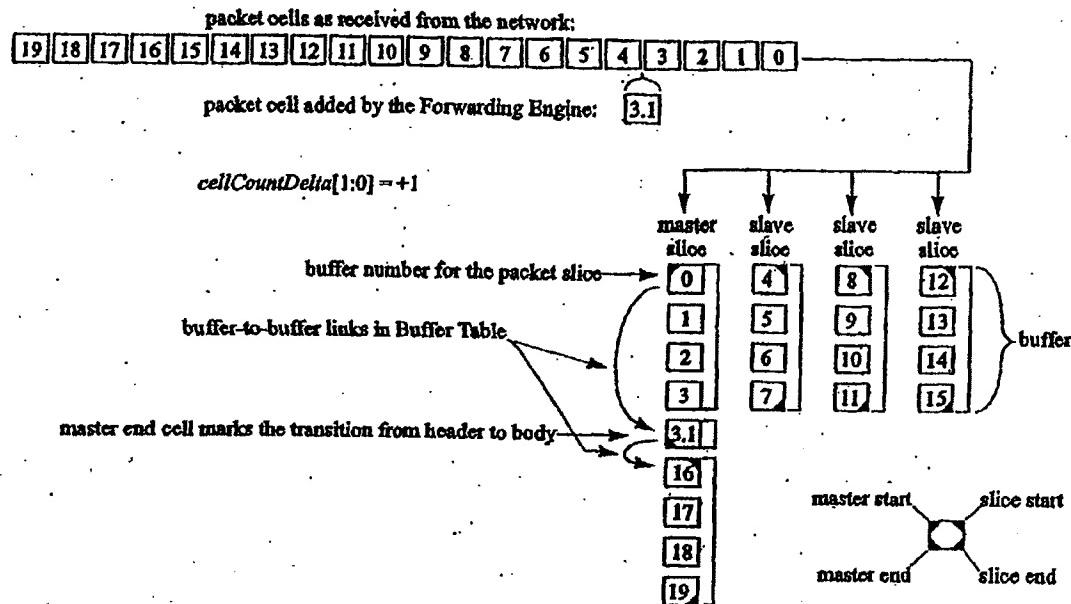
FIG. 9G



F16. 9 H

Header Expansion on Ingress Store

FIG. 10A



Header Expansion on Ingress Store with Post Storage Header Delivery

FIG. 10B

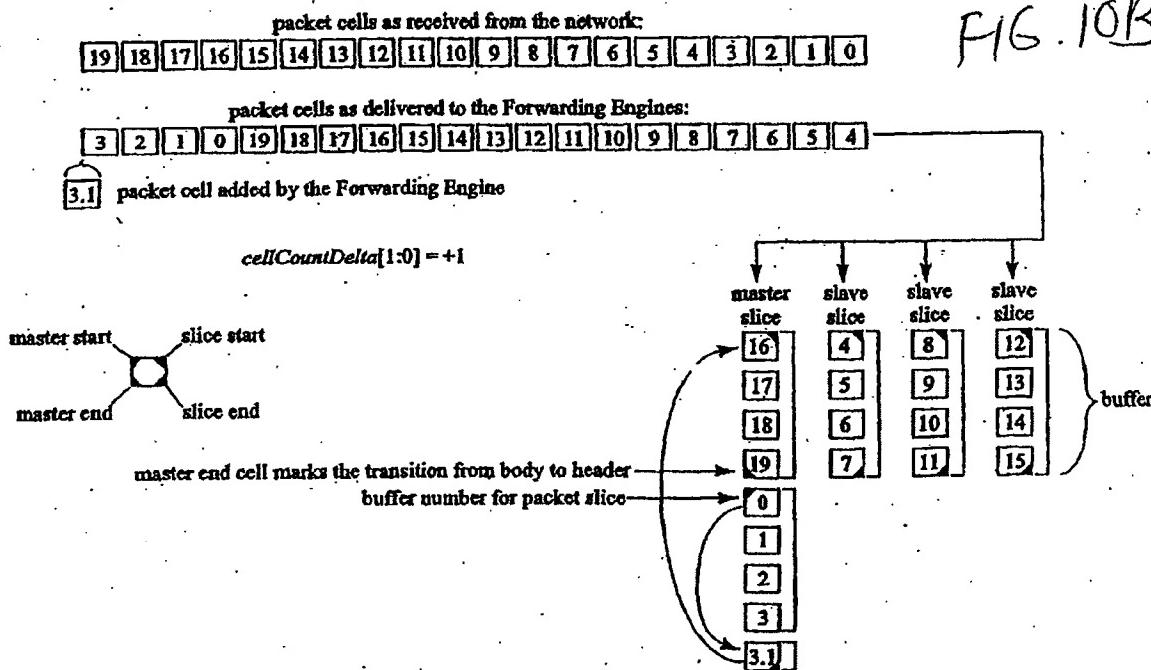


FIG. 10C

Cell Sequencing on Egress Store

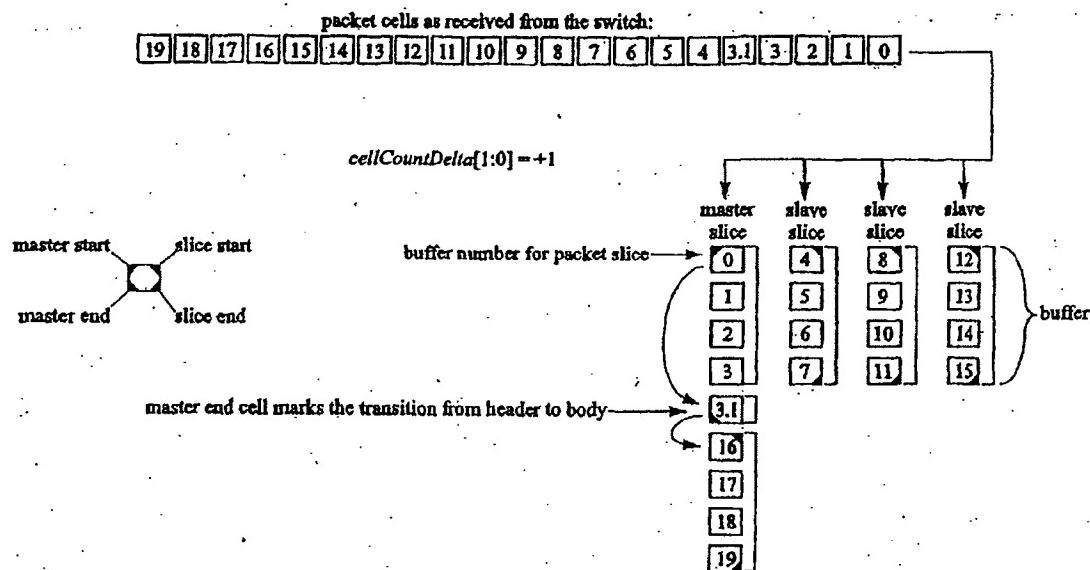


FIG. 10D

Cell Sequencing and Elasticity on Egress Retrieve

